Multilevel Pattern Generator PAT 1250-16

Key Features

- **Broadband pattern generator with 16-ary output signals**
- **Pattern generation from 10 up to 1250 MHz**
- **Freely programmable 32 MBit pattern memory**
- **Two independent output channels**
- **Latest technology using SiGe and InPh integrated circuits**
- **Easy-to-use graphical user interface on PC (via USB-port)**

Brief Description

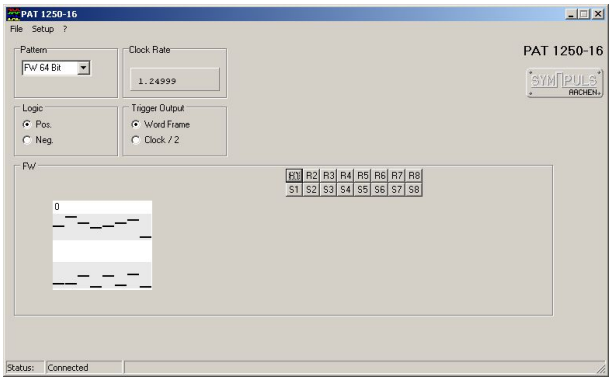
The multilevel pattern generator PAT1250-16 is a special generator for testing digital designs and components, e. g. laser diodes. The output signals use a multilevel signal code, i. e. they can adopt not only one of two (binary), but one out of sixteen possible voltage values. Every code element therefore is encoded using four bit.

Definition of a Digit A single code element or data character is referred to in the following as *digit*. A digit is encoded using four bit and can adopt 16 different voltage values. All steps between adjoining voltage values are equal.

For the operation of the generator an external reference clock signal in the range of 20 MHz to 2,5 GHz is required. Repetition rates with frequencies between 10 MHz and 1,25 GHz are possible.

The freely programmable internal 32 MBit pattern memory allows the generation of customized patterns of up to 4.194.304 data characters.

All signal outputs and inputs are accessible at the front panel. These are: reference clock input, two independent output signals (Multilevel A and Multilevel B), data clock output, quadrature clock signal (90° phase difference) and trigger output.



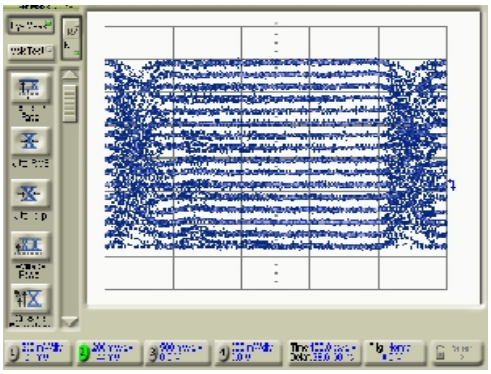
Graphical user interface of the operating software

SYMPULS GmbH
Römerstr. 39
D-52064 Aachen

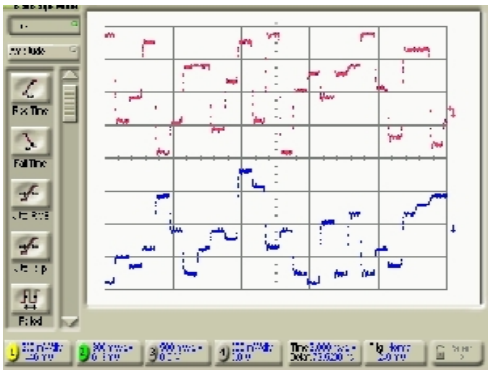
Tel: 0(049) 241 35334
Fax: 0(049) 241 35335

Internet: www.sympuls-aachen.de
Email: mail@sympuls-aachen.de

Output signals of the PAT 1250-16



Output signal A with statistical data distribution and data clock trigger



Output signals Multilevel A and B wordframe triggered

Technical Specifications

PAT 1250-16	
Data rate	10 . . . 1250 MHz
Clock input	20 . . . 2.500 MHz Reference clock input equals twice the data rate) $U_i = 0,5 \ldots 1\,V_{pp}, R_i = 50\,\Omega$, 50 Ω SMA, $\lvert r\rvert < 0,2$ 6-digit frequency indicator (on the GUI)
Data output	2 output channels with 16 amplitude levels each independently programmable, DC-coupled, amplitude ca. 1,2 V_{pp}, 50 Ω SMA
Pattern	Freely programmable pattern Word length variable: $8 * m$ digits ($m = 3 \ldots 219$) (= 24 . . . 4.194.304 digits), programmable via USB-port, reversible polarity
Memory	32 MBit (= 4.194.304 digits per channel)
Clock output	1) Data clock, $0,6\,V_{pp} \pm 0,2\,V_{pp}$, DC-free, SMA 2) Data clock − 90°, equals 1) with a phase difference of 90 ° (The data clock signal is derived from the reference clock signal using a frequency divider)
Interface	USB-port with a data rate of ca. 1 MByte/s
Measurements	19ttable housing, weight ca. 5 kg widht x height x depth = 462 x 90 x 315 mm
Power supply	230 V/50-60 Hz/32 VA

SYMPULS GmbH
Römerstr. 39
D-52064 Aachen

Tel: 0(049) 241 35334
Fax: 0(049) 241 35335

Internet: www.sympuls-aachen.de
Email: mail@sympuls-aachen.de