Pulse Pattern Generator PAT 5000

Key Features

- **Universal Pulse Pattern Generator for Test and Measurement Applications**
- **Gap-Free Operation over the Complete Frequency Range between 25 MHz and 5 GHz**
- **Internal Clock Generator**
- **PRBS and User Programmable Pattern of Variable Length up to 16 777 216 Bit**
- **Jitter-transparent for Jitter Tolerance Testing**
- **Operation via Front Panel or USB-Interface**

This wideband tuneable pulse pattern generator provides hardware-based pseudo random binary sequences and memory-based user programmable bit patterns. An internal clock source, adjustable output amplitude and offset levels and various pattern modes make the instrument adapted to a wide field of test and measurement applications. Fast signal transitions times below 70 ps and a RMS jitter under 3 ps assure good signal quality. In combination with the Error Analyzer SBF 3000 the pattern generator forms a complete bit error rate test set.

Clock Source

The clock source determines the time base for operation. All the output signals are derived from it. There are two main clock sources:

Internal

The internal quartz controlled clock generator provides clock signals in the range from 25 MHz to 5 GHz.

External

The clock signal connected to the instruments *Clock Input* is used as system clock. The clock input is jitter-transparent and the instrument follows even abrupt frequency changes of the externally attached signal.

10 MHz Reference Input

A 10 MHz reference clock signal can be applied to the reference clock input on the instruments rear panel. This clock signal is used as reference for all timing parameters.

10 MHz Reference Output

The 10 MHz reference clock output signal can be used to synchronize the time base of other instruments to the time base of the pattern generator.

Pattern

PRBS

Hardware generated pseudo random binary sequences of length between $2^7 - 1$ and $2^{31} - 1$ can be selected as pattern data.

PRBS	2^n-1, n=7, 9, 11, 15, 23, 31	
PRBS	Polynomial	Specification
2^7-1	X^7+X^6 +1	
2^9-1	X^9+X^5 +1	CCITT O.153/ITU-T O.153
2^{11}-1	$X^{11}+X^9$ +1	CCITT O.152/ITU-T O.152
2^{15}-1	$X^{15}+X^{14}$ +1	CCITT O.151/ITU-T O.151
2^{23}-1	$X^{23}+X^{18}$ +1	CCITT O.151/ITU-T O.151
2^{31}-1	$X^{31}+X^{28}$ +1	CCITT O.150/ITU-T O.150

Data

Arbitrary user pattern data up to a maximum length of 16 MBit can be generated.

Pulse Format

NRZ

Non-return to zero pulse format. The output signal remains at the low or high level according to the level of the selected bit pattern for the entire period of the selected clock source.

Output Modes

Pulse Pattern Mode

The selected bit pattern is repeated periodically.

Burst Mode

In burst mode the pattern generator generates a single burst signal. The pattern data is generated n times ($1 < n < 255$) followed by continuous zeros. The burst signal can be started by:

- applying a trigger signal to the AUX input
- sending the start command over the USB-interface.

Alternate Subpattern Mode

In this mode two subpatterns A and B of the same length can be generated alternately. Pattern A is generated i times followed by j repetitions of pattern B. Alternatively the AUX input can be used to toggle synchronously between patterns A and B. The alternate subpattern mode can also be used to generate repetitive signal bursts.

Data Polarity

The polarity of the output signals can be set to normal or inverted. If the polarity is set to inverted the low and high level bits are interchanged. In PRBS mode normal polarity corresponds to the PRBS pattern definitions according to CCITT specifications.

Bit Shift

With the bit shift functionality it is possible to delay the output signal by n bits to compensate for cable delays or to synchronize two data patterns at specific bit positions.

Figure 1: Output pattern at 3 Gbps delayed by 3 bits

Output Levels

The output levels can be set to custom values by adjusting output amplitude and offset.

Amplitude

The output amplitude is adjustable between 0.5 V_{pp} and 1 V_{pp}.

Offset

A DC-offset between -(Amplitude/2) and +(Amplitude/2) can be added to the output signal.

Error Insertion

Programmable Error Addition

The error addition allows to add errors to the output data stream. Error rates between 10^{-4} and 10^{-10} and single error mode are selectable. Exactly one bit is inverted, e. g. if the error rate 10^{-9} is selected, one out of 10^9 bits will be inverted.

Error Input

The error input accepts a TTL signal. With every transition of the signal connected to the error input an error is added to the output data stream.

Trigger Signals

Trigger Output

The trigger output provides a divided clock signal or a pattern synchronous trigger signal.

Clock Output

The clock output provides a clock signal of the frequency identical to the system clock frequency. It can be additionally divided by n ($n = 1, 2, 4, 8$).

Aux Input

Depending on the selected output mode the AUX input has different functionality. It may be used to trigger signal bursts or toggle synchronously between two subpatterns.

Jitter Insertion

When the external clock input is used the pattern generator follows exactly the externally connected frequency. By modulating the external clock source jitter-modulated data signals can be generated. Optionally the PAT 5000 is also available with an internal time delay. By applying a modulation signal to the delay control input various shapes of signal jitter can be generated.

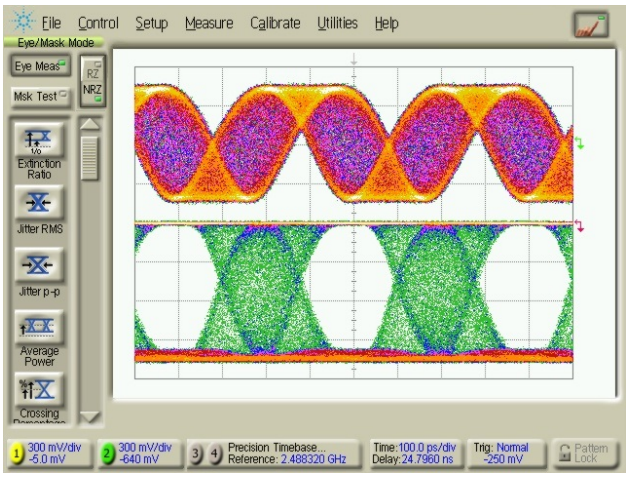

Figure 2: Jitter modulated with sine-wave: Clock Input and Data Output Signal at 2.4883 Gbps

Front Panel Controls

All instrument settings can be changed using the navigation keys on the front panel. The device parameters are accessible through an intuitive menu structure that is displayed on the front.

Graphical User Interface

The graphical user interface allows to change all device settings, program the user pattern and set the internal clock rate by simple mouse-clicking. The last settings are automatically saved when power is turned off.

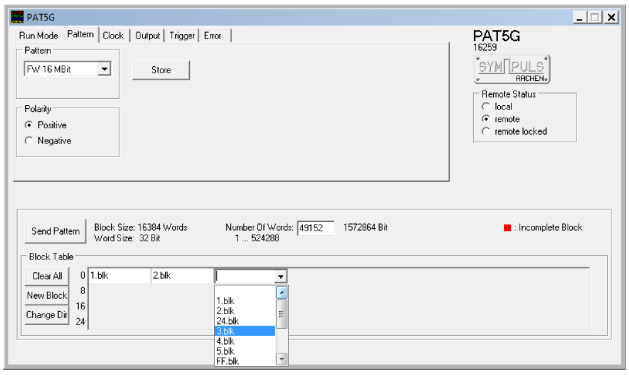

Figure 3: Graphial User Interface of the Operating Software

Technical Specifications

Bit Pattern Generator PAT 5000	
Internal Clock	
Quartz Controlled Clock Generator	
Frequency Range	25 MHz ... 5000 MHz
Frequency Resolution	100 kHz
10 MHz Reference Input	$U_i = 1\,V_{pp} \ldots 3\,V_{pp}$ 50 Ω SMA, AC-coupled
10 MHz Reference Output	Amplitude $1.5\,V_{pp}$ 50 Ω SMA, AC-coupled
External Clock	
Frequency Range	10 MHz ... 5000 MHz
Impedance	$R_i = 50\,\Omega$, $\lvert r\rvert < 0,2$
Input Amplitude	$U_i = 0,5 \ldots 1,0\,V_{pp}$,
Connector	50 Ω SMA
Pattern Generation	
Data Format	Non-return to zero
Data Rate	According to Input Clock, 10 Mbps ... 5 Gbps
PRBS	$2^{31}-1$, $2^{23}-1$, $2^{15}-1$, $2^{11}-1$, 2^9-1, 2^7-1
Pattern Memory	16 777 216 Bit
Programmable Pattern Length	$32 * m$ Bit $(m = 1, 2, 3, \ldots, 2^{19})$
Data Outputs	
Complementary data outputs NRZ and /NRZ, DC-coupled	
Amplitude	$0.5\,V_{pp} \ldots 1\,V_{pp}$ into 50 Ω
Offset	± (Amplitude/2), max. ± 500 mV
Rise/Falltime (20%-80%)	< 30 ps
Jitter (pp)	< 12 ps
Duty Cycle	50% Nominal
Data Polarity	Normal or Inverted Logic
Impedance	$R_i = 50\,\Omega$, $\lvert r\rvert < 0.2$
Connector	50 Ω SMA, $\lvert r\rvert < 0.2$
Clock Outputs	
Complementary clock outputs Clock and /Clock, AC-coupled	
Frequency Divider	1, 2, 4 and 8
Amplitude	$0.8\,V_{pp} \pm 0.2\,V$
Rise/Falltime (20%-80%)	< 50 ps
Data to Clock Skew	± 50 ps
Connector	50 Ω SMA

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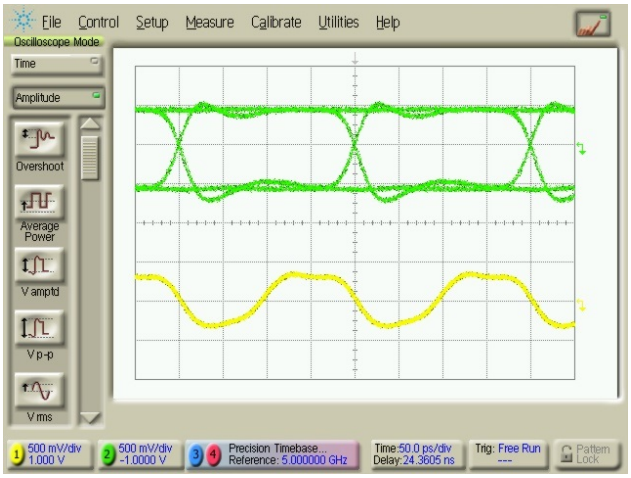
Trigger Output	
Trigger Modes	1. Clock/32 2. Word Frame Trigger (Data Synchronous Trigger)
Amplitude	$(-0.4\,V \pm 0.1\,V)/0\,V$, DC Coupled
Connector	$50\,\Omega$ SMA, $\lvert r\rvert < 0.2$
Error Insertion	
Programmable Error Addition	Single, $10^{-4}, 10^{-5}, \ldots, 10^{-10}$
AUX Input	TTL Input, $U_i = 0.1\,V \ldots 5\,V$, Programmable Threshold Voltage 50 mV ... 4000 mV, Maximum Error Frequency $\leq$ (Data Rate)/100
General Information	
Interface	Operation via Front Panel or High Speed USB Data Transfer Rate up to 6 MByte/s
Dimensions	10” Desktop W x H x D = 256 x 80 x 264 mm^3
Weight	approx. 2 kg
Power Supply	115 V/230 V/50-60 Hz/20 VA

Output Signals

All oscillograms in this section were taken using the Agilent 86100B sampling oscilloscope and the sampling module 86118A (70 GHz cut-off frequency).

Typical Output Waveforms

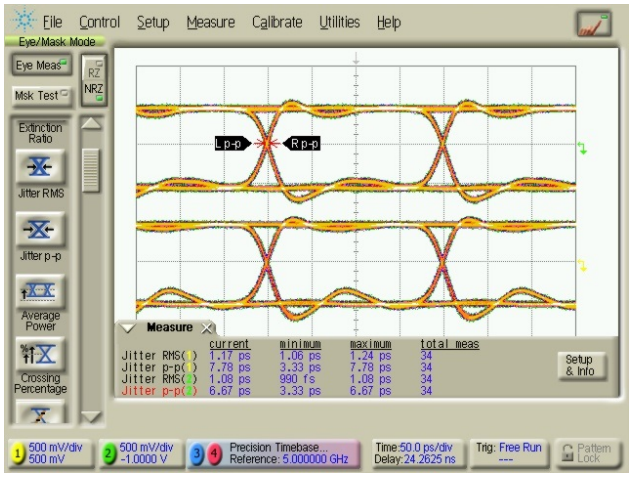
(a) PRBS $2^7 - 1$ at 5 Gbps



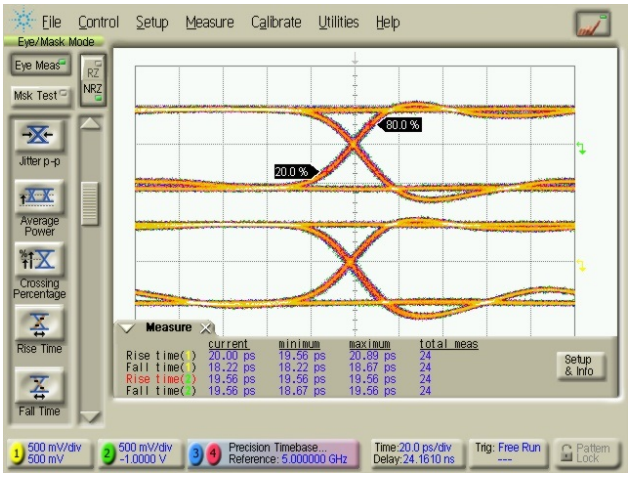
(b) Clock and Data Outputs at 5 Gbps

Figure 4: Typical Output Waveforms

Jitter and Transition Times



(a) Jitter of the Data Outputs at 5 Gbps



(b) Rise- and Falltimes at 5 Gbps

Figure 5: Jitter and Transition Times of the Data Outputs

Ordering Information

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Included in delivery:

PAT 5000

- Mainframe with SMA Connectors
- User Manual, USB Cable
- CD-ROM with Device Drivers and Operating Software

The instrument is produced by SYMPULS in Germany.
We offer a reliable service and 24 month warranty.