

Pulse Pattern Generator BPG 40G



Key Features

- **Universal Pulse Pattern Generator for Test and Measurement Applications with Complementary Data Outputs**
- **Gap-Free Operation at Data Rates between 400 Mbps and 40 Gbps**
- **PRBS and User Programmable Pattern of Variable Length up to 256 MBit**
- **Jitter-transparent for Jitter Tolerance Testing**
- **Operation via Front Panel or USB-Interface**
- **Optionally Available:**
 - **Internal Clock Generator**
 - **Extended Pattern Memory up to 1 GBit**
 - **Sub-Channel Outputs 2x20 Gbps**

This wideband tuneable pulse pattern generator provides hardware-based pseudo random binary sequences and memory-based user programmable bit patterns at data rates between 500 Mbps and 40 Gbps. The generator is jitter-transparent and follows even abrupt frequency changes. Optionally available internal clock source, adjustable output amplitude and various pattern modes make the instrument adapted to a wide field of test and measurement applications. Fast signal transitions times below 12 ps (typically) and a RMS jitter under 1 ps assure good signal quality. In combination with the Error Analyzer SBF 40G

the pattern generator forms a complete bit error rate test set.

Clock Source

The clock source determines the time base for operation. All output signals are derived from it. The pattern generator is operated with a clock signal of half the output data rate, i.e. with a clock signal of 20 GHz the instrument generates output patterns at 40 Gbps. Optionally the instrument is available with a full-clock input and internal divider. There are two main clock sources:

Internal Synthesizer

The internal quartz controlled clock generator provides clock signals in the range from 200 MHz to 20 GHz corresponding to output data rates between 400 Mbps and 40 Gbps.

External Clock Input

The clock signal connected to the instruments *Clock Input* is used as system clock. The clock input is jitter-transparent and the instrument follows even abrupt frequency changes of the externally attached signal. All instrument modes are available in both internal and external clock mode.

10 MHz Reference Input

A 10 MHz reference clock signal can be applied to the reference clock input on the instruments rear panel. This clock signal is used as reference for all timing parameters.

10 MHz Reference Output

The 10 MHz reference clock output signal can be used to synchronize the time base of other instruments to the time base of the pattern generator.

Clock Output

The differential clock output provides a clock signal of half the output data rate, i.e. 20 GHz at a data rate of 40 Gbps, according to the selected input clock signal. The CML output signal is AC-coupled and has amplitude of $400 mV_{pp} \pm 100 mV_{pp}$ into 50Ω .

Pattern

PRBS

Hardware generated pseudo random binary sequences of length between $2^7 - 1$ and $2^{31} - 1$ can be selected as pattern data.

PRBS	$2^n - 1, n=7, 9, 11, 15, 23, 31$	
PRBS	Polynomial	Specification
$2^7 - 1$	$X^7 + X^6 + 1$	
$2^9 - 1$	$X^9 + X^5 + 1$	CCITT O.153/ITU-T O.153
$2^{11} - 1$	$X^{11} + X^9 + 1$	CCITT O.152/ITU-T O.152
$2^{15} - 1$	$X^{15} + X^{14} + 1$	CCITT O.151/ITU-T O.151
$2^{23} - 1$	$X^{23} + X^{18} + 1$	CCITT O.151/ITU-T O.151
$2^{31} - 1$	$X^{31} + X^{28} + 1$	CCITT O.150/ITU-T O.150

Pseudo random binary sequences of length up to $2^{20} - 1$ can be generated by loading the corresponding pattern data into the pattern memory of the generator.

Data

Arbitrary user pattern data up to a maximum length of 256 MBit can be generated. The pattern length can be set in steps of 256 bits. The programmed bit sequence is generated periodically. Additionally the pattern memory can be split in 2 or 4 parts to toggle synchronously between different waveforms. Optionally the pattern generator is available with an extended pattern memory of 512 MBit or 1024 MBit.

Pulse Format

NRZ

Non-return to zero pulse format. The output signal remains at the low or high level according to the level of the selected bit pattern for the entire period of the selected clock source.

Data Polarity

The polarity of the output signals can be set to normal or inverted. If the polarity is set to inverted the low and high level bits are interchanged. In PRBS mode normal polarity corresponds to the PRBS pattern definitions according to CCITT specifications.

Output Amplitude

The instrument generates signals with negative output levels of $-U_{peak}$ and 0 V. U_{peak} is adjustable between 0.3 V and 0.6 V with a resolution of 1 mV.

Error Insertion

Programmable Error Addition

The error addition allows to add errors to the output data stream. Error rates between 10^{-4} and 10^{-10} and single error mode are selectable. Exactly one bit is inverted, e.g. if the error rate 10^{-9} is selected, one out of 10^9 bits will be inverted.

AUX Input

The AUX input has an adjustable input threshold between -4000 mV and +4000 mV and accepts signals with a maximum amplitude of $5 V_{pp}$. With every transition of the signal connected to the AUX input an error is added to the output data stream.

Jitter Insertion

When the external clock input is used the pattern generator follows exactly the externally connected frequency. By modulating the external clock source jitter-modulated data signals can be generated.

Trigger Signals

Trigger Output

The trigger output can be switched between the divided clock signal (Bit Rate)/32 and a pattern synchronous trigger signal (wordframe trigger signal).

Front Panel Controls

All instrument settings can be changed using the buttons on the front panel. The device parameters are accessible through an intuitive menu structure that is displayed on the LCD.

Graphical User Interface

The graphical user interface allows to change all device settings and program the user pattern by simple mouse-clicking. The last settings are automatically saved when power is turned off.

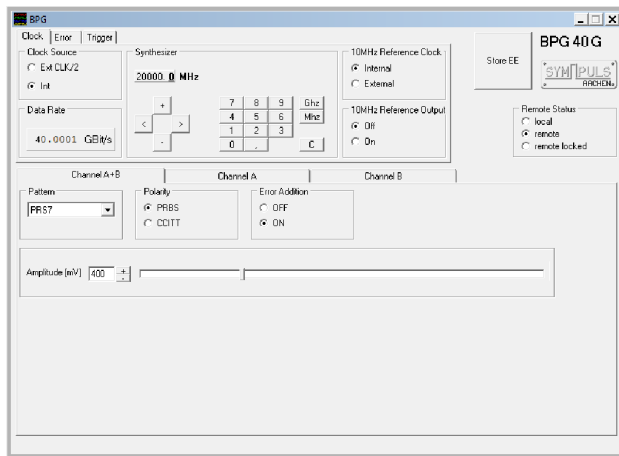


Figure 1: Graphical User Interface of the Operating Software

SCPI Remote Control

The pattern generator can be remotely controlled via SCPI commands, a standardized instruction set for controlling and programming measurement instruments. The SCPI commands are transferred to the instrument in ASCII text format and may be generated using any programming language and development environment.

Options

Full-Clock Input

The integrated divider allows to connect clock signals of the full output data rate, i.e. 40 GHz for 40 Gbps output data signals. The clock input can be switched over from *full-clock* mode to *half-clock* mode.

Differential 20 Gbps Data Outputs

The two 20 Gbps sub-channels used for generating the 40 Gbps output signal of the instrument are available at additional front panel outputs and may be used for generating higher-order modulation signals. The generator can be used alternatively in *sub-channel mode* or in *multiplex mode*. In *sub-channel mode* the all settings for the two sub-channels can be programmed independently. The output amplitude is always independently adjustable between $0.25 V_{pp}$ and $0.5 V_{pp}$. Additionally the sub-channels may be delayed separately by $\pm 15 ps$, e.g. to compensate for different propagation times of connecting cables.

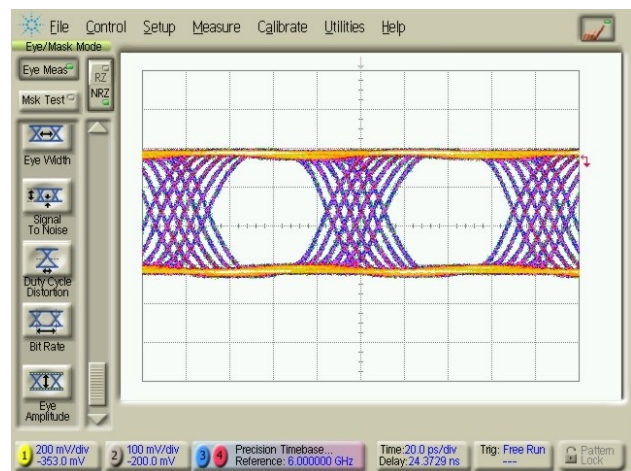


Figure 2: Example of an output signal delayed in steps of 5 ps

Bit Shift

IN PRBS mode the bit shift functionality allows to delay the output signal by n bits ($0 \leq n \leq 2147482645$) to compensate for cable delays or to synchronize the two subchannel patterns at specific bit positions.



Figure 3: Example of a PRBS signal delayed by 3 bits

Technical Specifications

BPG 40G	
External Clock	
Frequency Range	500 MHz ... 20 GHz (External Clock Rate = (Data Rate)/2 6-digit frequency display
Input Amplitude	$U_i = 0.5 \dots 1.0 V_{pp} (-3 dBm \dots + 3 dBm)$,
Impedance	$R_i = 50 \Omega, r < 0, 2$
Connector	50 Ω 2.92 mm (K)
Pattern Generation	
Data Format	NRZ
Data Rate	According to input clock frequency, 1 Gbps ... 40 Gbps
PRBS	$2^{31} - 1, 2^{23} - 1, 2^{15} - 1, 2^{11} - 1, 2^9 - 1, 2^7 - 1$
Programmable Patterns	<ol style="list-style-type: none"> 1. User Programmable Patterns of 16 and 256 Bit Length, Manually Programmable via Front Panel 3. User Patterns of Length $256 * m$ Bit ($m = 1, 2, \dots, 2^{20}$) (=max. 268 435 456 Bits), Programmable via USB-Port 4. User Patterns Consisting of Two Parts, Each of Length $256 * m$ Bit ($m = 1, 2, \dots, 2^{19}$), Programmable and Synchronously Selectable via USB-Port (Two Waveform Mode) 5. User Patterns Consisting of Four Parts, Each of Length $256 * m$ Bit ($m = 1, 2, \dots, 2^{18}$), Programmable and Synchronously Selectable via USB-Port (Four Waveform Mode)
Pattern Memory	268 435 456 Bits
Programmable Pattern Length	$256 * m$ bits, ($m = 1, 2, 3, \dots, 2^{20}$)
Long user patterns only programmable via the instruments USB interface	
Data Outputs	
Complementary data outputs Data and /Data, DC-coupled	
Amplitude	$(-600 mV \dots - 300 mV)/0 V$ into 50 Ω
Amplitude Resolution	1 mV
Rise/Falltime (10%-90%)	< 13 ps
Jitter (rms)	< 1 ps
Duty Cycle	50% \pm 2.5 %
Data Polarity	Normal or inverted logic
Connector	50 Ω 2.92 mm (K), $ r < 0.2$

BPG 40G

Clock Outputs

Complementary clock outputs Clock and /Clock, AC-coupled

Amplitude $0.4 V_{pp} \pm 0.1 V_{pp}$ into 50Ω

Connector 50Ω 2.92 mm (K), $|r| < 0.2$

Trigger Output

Trigger Modes

1. Bit Rate/32,
2. Word frame trigger (Data synchronous trigger)

Amplitude $0.4 V_{pp} \pm 0.1 V$ into 50Ω , DC Coupled

Connector 50Ω SMA, $|r| < 0.2$

Error Insertion

Programmable Error Addition Single, 10^{-4} , 10^{-5} , ..., 10^{-10}

AUX Input

Input Voltage Max. $\pm 10 V$,

Impedance $1 k\Omega$

Input Swing $100 mV_{pp} \dots 5 V_{pp}$

Input Threshold $-4000 mV \dots 4000 mV$, Resolution $10 mV$

General Information

Interface High-speed USB
Data Transfer Rate up to 10 MByte/s

Software Graphical User Interface for Operation and Pattern Programming

Dimensions 19" Desktop
W x H x D = 462 x 135 x 435 mm³

Weight approx. 8 kg

Power Supply $100 V - 240 V/50 Hz - 60 Hz/90 VA$

Options

Option 1: Extended Memory 512 MBit

Pattern Memory	536 870 912 Bits
Pattern Length	$256 * m$ Bits, ($m = 1, 2, \dots, 2^{21}$)

Option 2: Extended Memory 1024 MBit

Pattern Memory	1 073 741 824 Bits
Pattern Length	$256 * m$ Bits, ($m = 1, 2, \dots, 2^{22}$)

Option 3: Full-clock Input

Input Frequency	1 GHz ... 40 GHz (External Clock Rate = Data Rate) <i>Full-clock</i> and <i>half-clock</i> input selectable
-----------------	--

Option 4: Internal Clock

Quartz controlled clock generator

Frequency Range	200 MHz ... 20 GHz
Frequency Resolution	5 Hz
10 MHz Reference Input	$U_i = 1 V_{pp} \dots 3 V_{pp}$ 50 Ω SMA, AC-coupled
10 MHz Reference Output	Amplitude $1.5 V_{pp}$ 50 Ω SMA, AC-coupled

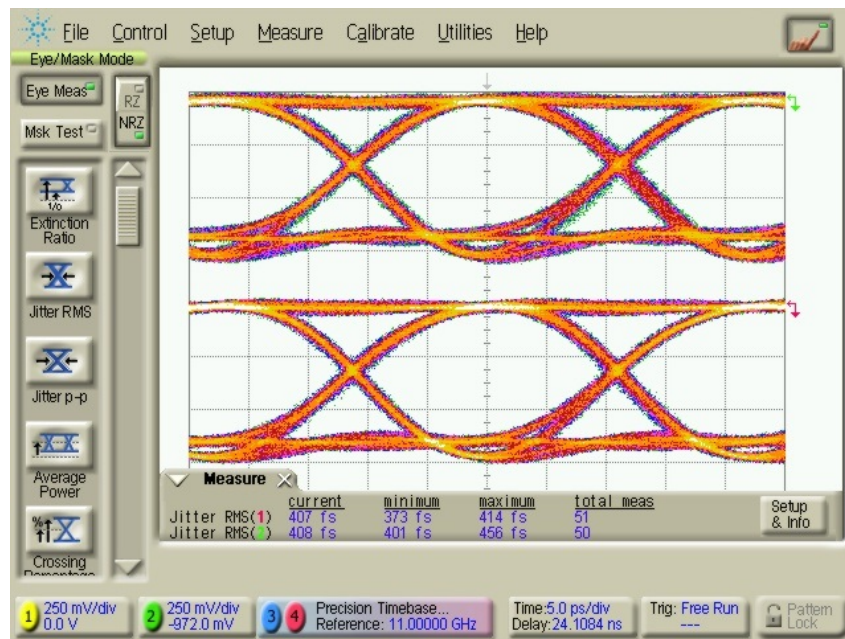
Option 5: Differential 20 Gbps Sub-channel Outputs

Data Format	NRZ
Data Rate	According to input clock frequency, 500 MBit/s ... 20 GBit/s
Amplitude	$(-0.5 V \dots -0.25 V)/0 V$ into 50 Ω
Rise-/Falltimes (20%-80%)	< 20 ps
Jitter (rms)	< 1 ps
Duty Cycle	$50\% \pm 2,5\%$
Bit Shift	max. 2 147 482 645 bits (in PRBS mode)
Delay	$\pm 15 ps$
Connectors	50 Ω SMA, $ r < 0,2$

Output Signals

All oscillograms in this section were taken using the Agilent 86100B sampling oscilloscope and the sampling module 86118A (70 GHz cut-off frequency).

Typical Output Waveforms



Differential Outputs at 44 Gbps

Ordering Information

SYMPULS GmbH

Römerstr. 39
D-52064 Aachen

Phone: +49 241 35334

Fax: +49 241 35335

Email: mail@sympuls-aachen.de

Internet: www.sympuls-aachen.de

Included in delivery:

- BPG 40G
- 115/230 V Mains, User Manual, USB Cable Set
- CD-ROM with Device Driver and Operating Software

**The instrument is produced by SYMPULS in Germany.
We offer a reliable service and 24 month warranty.**